ABSTRACT OF THE DISCLOSURE

A gate insulating layer, an amorphous silicon layer, an n^+ amorphous silicon layer and a metal layer are deposited in sequence after a gate line, a gate electrode and a gate pad are formed on a substrate, using a first mask. The metal layer is etched to form a data line, a source electrode, a drain electrode and a data pad through a photolithography process, using a second mask, and the n^+ amorphous silicon layer is etched, using the patterned data line, the source electrode, the drain electrode and the data pad as the mask. A light shielding film and a passivation film, or a passivation film also having a function of the light shielding film are deposited, and is etched through the photolithography process, using a third mask which leaves a portion covering the gate line, the gate electrode, the gate pad and the data line, the source electrode, and the drain electrode. The amorphous silicon layer and the gate insulating layer are etched, using the patterned light shielding film and passivation film, or the patterned passivation film also having the function of the light shielding film as the mask. Here, the gate pad, the data pad and a part of the drain electrode are exposed. A pixel electrode connected to the drain electrode, is formed and indium tin oxide (ITO) pads covering the exposed gate pad and the exposed data pad, is formed by depositing an ITO film and etching thorough the photolithography, using a fourth mask. As a result, a thin film transistor

array panel used for a liquid crystal display is fabricated by only four masks.